INFO: [VRFC 10-2263] Analyzing Verilog file "C:/Users/eacm3/Desktop/project\_3/project\_3.sim/sim\_1/impl/timing/xsim/Testbench\_full\_adder\_time\_impl.v" into library xil\_defaultlib

INFO: [VRFC 10-311] analyzing module full\_adder

INFO: [VRFC 10-311] analyzing module glbl